REMARKS/ARGUMENTS

Claim Rejections – 35 USC § 103. The Office Action rejected claims 1-5, 8-14, 16-18 and 20 under Section 103(a) of the U.S. Patent Act as being unpatentable over "Applicant's Admitted Prior Art" (APA) set forth in paragraphs [0002] through [0004] of the specification and Surti et al. (U.S. Patent No. 6,496,193). The Office Action further rejected claims 6, 7, 15, and 19 under Section 103(a) as being unpatentable over the combined teachings of Applicant's APA and Surti et al. in view of Saxena et al. (U.S. Patent Publication No. 2003/0122837). Applicant respectfully traverses these rejections because none of these cited references discloses or suggests a tile converter in communication with the system memory for converting image data into tiled mode and storing the tiled data into the system memory.

As stated in paragraph 4 of the Office Action (page 3), the APA does not expressly teach a second tile converter in communication with the core logic unit for converting the first image data into fourth image data in a tile mode and system memory accessible by the core logic unit and comprising a graphics accelerating memory in communication with the second tile converter for storing therein the fourth image data. Claim 1 recites that the core logic unit outputs first image data in a linear mode. According to the Office Action, the Surti et al. patent discloses these features.

Surti et al. discloses that graphics memory and system memory are both arranged as tiled memories. Column 3, lines 23-25. Storing data in a tiled memory and converting linear data into titled mode for storage in normal memory are distinctly different operations. It can reasonably be inferred by persons having ordinary skill in the art that Surti does not disclose or suggest a tile converter arranged upstream of the system memory for doing tile conversion. The conversion of the virtual addresses in Surti, on the other hand, is an operation within the memory rather than an upstream converter.

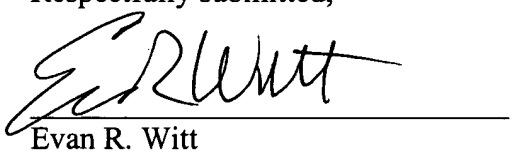
To tile a memory, as understood by persons having ordinary skill in the art, means to change the allocation mechanism of the memory. Since a system memory is a shared device for various objectives, and the graphics accelerating memory just occupies a portion of the system memory, the Applicant believes it would be unwise to use a titled memory as a system memory. Instead, the present invention uses a tile converter in communication with the graphics

accelerating memory in the system memory to achieve the purpose of storing titled data without the need of changing the allocation of any memory. Accordingly, Applicant submits that the rejected claims 1-5, 8-14, 16-18 and 20 would not have been obvious from the combined teachings of APA and Surti et al. Withdrawal of the rejection is respectfully requested.

Like Surti et al., Saxena et al. discloses a tiled memory. Saxena et al.'s invention is drawn to a method and apparatus for optimally mapping a tiled memory surface to two memory channels operating in an interleaved fashion. The Saxena et al. patent does not disclose or suggest a tile converter in communication with the system memory for converting image data into tiled mode and storing the tiled data into the system memory. Accordingly, Applicant submits that the rejected claims 6, 7, 15, and 19 would not have been obvious from the combined teachings of APA, Surti et al., and Saxena et al. Withdrawal of the rejection is respectfully requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case. If there are any remaining issues preventing allowance of the pending claims that may be clarified by telephone, the Examiner is requested to call the undersigned.

Respectfully submitted,



Evan R. Witt
Reg. No. 32,512
Attorney for Applicant(s)

Date: June 13, 2005

MADSON & METCALF
Gateway Tower West
15 West South Temple, Suite 900
Salt Lake City, Utah 84101
Telephone: 801/537-1700